

## ABSTRACT

An apparatus including a content addressable memory (CAM) array, a clocked circuit coupled to the CAM array, and a programmable delay circuit coupled to receive a reference clock signal and generate a programmable delayed clock signal using a delay element for the clocked circuit. The CAM array may include a plurality of rows of CAM cells each having a corresponding match line for carrying a match signal indicative of whether comparand data matches data of the corresponding row of CAM cells.